MQEG4D1-DMC-8VT1

Features

- Support 400G bps aggregate bit rates
- Up to 53.125G bps Data rate per channel
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF
- 2-wire interface with integrated Digital Diagnostic Monitoring
- Case operating temperature range:0°C to 70°C
- Power dissipation <9 W
- Electrically hot-pluggable
- Single MPO connector receptacle

Applications

- 400GBASE-SR8 400G Ethernet
- Data center

Standards

- Compliant with QSFP-DD MSA
- Compliant with IEEE 802.3CD
- RoHS Compliant

General Description

MNC MQEG4D1-DMC-8VT1 are designed for use in 400Gbps links over multimode fiber. They are compliant with the QSFP-DD MSA.

The optical transmitter portion of the transceiver incorporates a 8-channel VCSEL array, a 8-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. For module control, the control interface incorporates a Two Wire Serial interface of clock and data signals. Diagnostic monitorsfor VCSEL bias, module temperature, TX power，RX power and supply voltage are implemented and results are available through the Two Wire Serial interface. Alarm and warning thresholds are established forthe monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. All flags are latched and will remain set even if the condition initiatingthe latch clears and operation resumes. The optical output will squelch for loss ofinput signal unless squelch is disabled.

The optical receiver portion of the transceiver incorporates a 8-channel PIN photodiode array, a 8-channel TIA array, a 8 channel output buffer, diagnostic monitors, and control and bias blocks.Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. All flags are latched and will remainset even if the condition initiating the flag clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through Two Wire Serial interface.

Specification

Absolute Maximum Ratings						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Storage Temperature	Ts	-40	-	85	ºC	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	

Recommended Operating Conditions						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Case Operating Temperature	Tcase	0	-	70	ºC	Without air flow
Power Supply Voltage	VCC	3.14	3.3	3.46	V	
Power Supply Current	ICC	-		2730	mA	
Data Rate	BR		53.125		Gbps	Each channel
Transmission Distance	TD		-	100	m	OM4 MMF

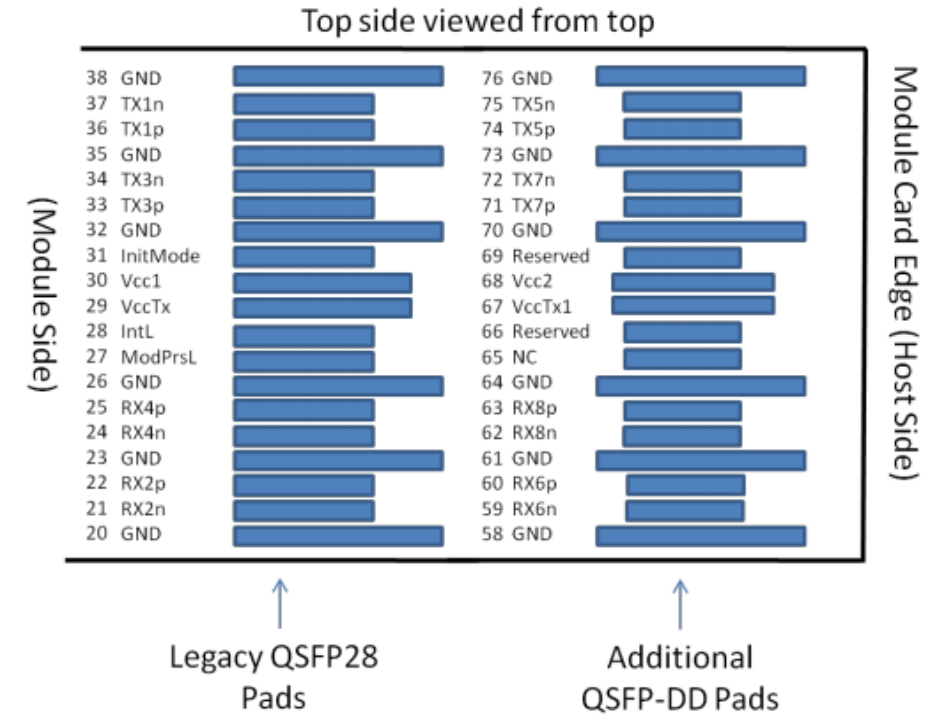
Optical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**NOTE**
Transmitter						
Modulation format	PAM4					
Signaling rate, each lane (range)		-100ppm	26.5625	+100ppm	GBd	
Center Wavelength	λ 0	840		860	nm	
Outer Optical Modulation Amplitude (OMAouter), each lane (max)				3		
Outer Optical Modulation Amplitude (OMAouter), each lane (min)		-4.5				1
Average Launch Power each lane		-6.5		4	dBm	

Spectral Width (RMS)	σ			0.6	nm	2
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	TDECQ			4.5	dB	
Optical Extinction Ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane (max)				-30	dBm	
Optical Return Loss Tolerance	ORL			12	dB	
Receiver						
Modulation format	PAM4					
Receiver Wavelength	λ in	840		860	nm	
Average receive power, each lane (max)				4	dBm	
Average receive power, each lane (min)		-8.4			dBm	3
Damage thresholda (min)		5			dBm	4
Receiver sensitivity (OMAouter), each laned (max)	RS = max (-6.5 , SECQ – 7.9)				dB	
Stressed receiver sensitivity (OMA) each lane	RSENS			-3.4	dBm	5
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test			4.5		dB	
OMA outer of each aggressor lane			3		dBm	
Receiver Reflectance	Rr			-12	dB	

Notes:

1. Even if the TDECQ < 1.4 dB, the OMA (min) must exceed this value.
2. RMS spectral width is the standard deviation of the spectrum.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Assignment



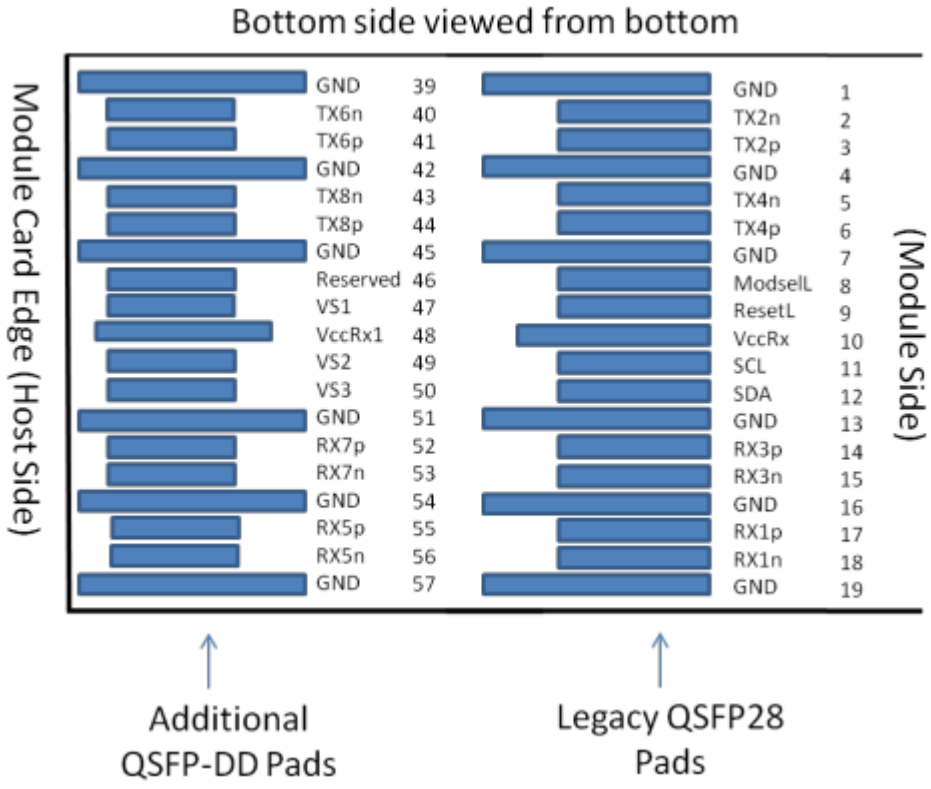


Table 1---Pad Function Definition

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All arecommon within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signalcommon ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently.Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Host - Transceiver Interface Block Diagram

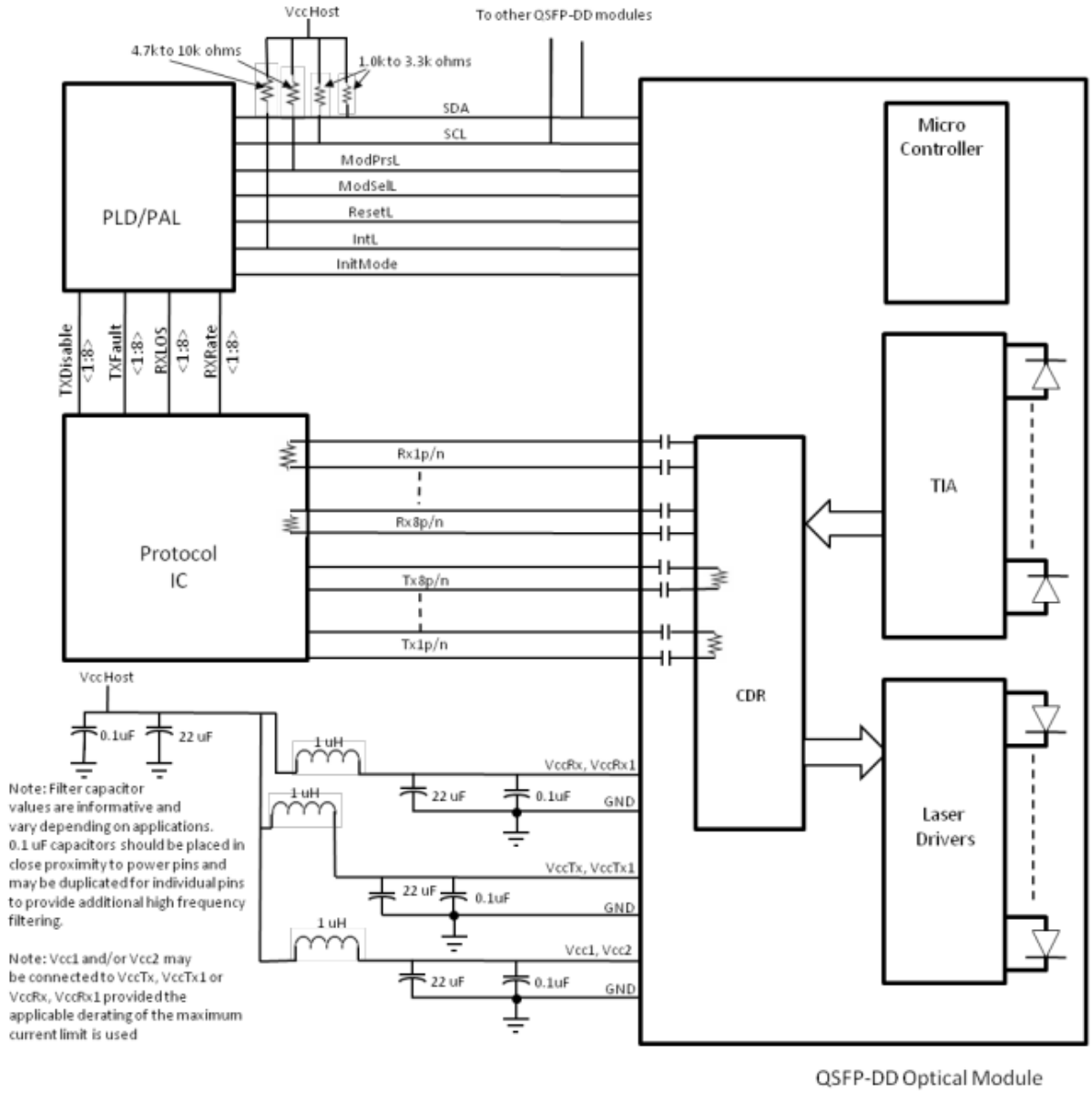
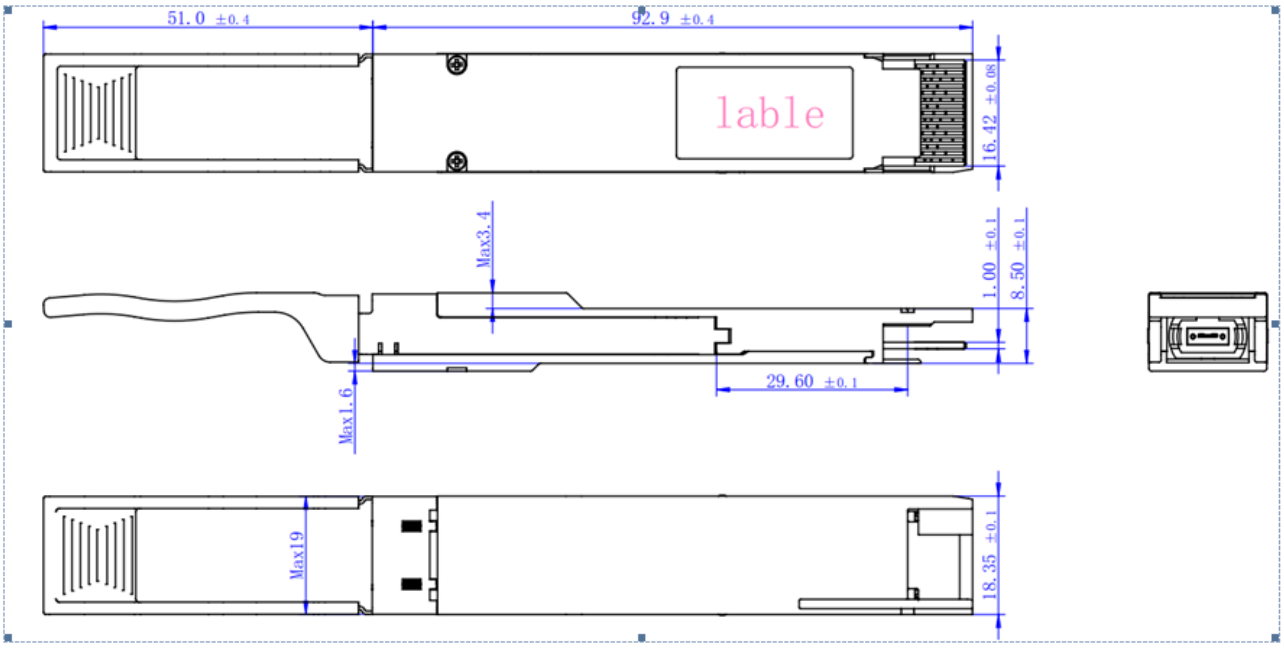


Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules

Package Outline



Ordering information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (m)	DDM
MQEG4D1-DMC-8VT1	QSFP-DD	400	850	-6.5~4	PIN	＜-3.4	0~70	100	Y